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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,538	11/14/2003	Roberto Bez	2110-62-3	7956

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EXAMINER	
SMITH, BRADLEY	
ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
04/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,538	BEZ ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,20,22,23,26-29,31,33-39 and 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20,22,23,26-29,31,33-39 and 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/27/08,12/31/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19, 20, 22, 23 26-29,31,33, 34-39 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et al. (US Patent 6,448,606). Yu et al. disclose a semiconductor body having a substrate; a pair of insulation structures (316, 317 and 318) disposed in the substrate, delimiting an active area of the substrate, and each having a respective portion projecting from said substrate, the projecting portions defining a recess over a portion of the active area and over a portion of at least one of the insulation structures; and a memory cell having a body region disposed in the portion of the active area, a gate insulator disposed over the body region (306), a floating gate (308) disposed in the recess over the gate insulator and over the portion of the at least one insulation structure such that the floating gate does not extend above the projecting portions of the insulating structures, and a control gate (312) disposed over the floating gate (308) (see figure 7c). Regarding claim 20, Yu et al. disclose projecting portions define the recess over respective portions of both of the insulation structures; and said floating gate (308) is disposed over the respective portions of both the insulating structures (see figure 7c). Regarding claim 22, Yu et al. disclose the floating gate (308) does not extend laterally beyond the projecting portions of the insulating structures (see figure 7c). Regarding claim 23, Yu et al. disclose floating gate has a surface facing the control gate, the entire surface being planar.

Regarding claim 26 , Yu et al. disclose a substrate having an active region; first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region and over a portion of at least one of the first and second insulators; a body region of the memory cell disposed in the portion of the active region; a first gate insulator (306) disposed over the body region; and a floating gate (308) of the memory cell disposed in the recess over the gate insulator and over the portion of at least one of the first and second insulators but not extending beyond the recess in a dimension parallel to a surface of the active region (see figure 7c). Regarding claim 27 , Yu et al. disclose the first and second insulators (316-318) respectively comprise first and second projections that define the recess (see figure 7c). Regarding claim 28 , Yu et al. disclose first and second trenches disposed in the substrate; and wherein the first and second insulators are respectively disposed in the first and second trenches (see figure 7c). Regarding claim 29, Yu et al. disclose wherein the first and second insulators define the recess over respective portions of both the first and second insulators(see figure 7c). Regarding claim 31 , Yu et al. disclose the floating gate does not extend above the first and second insulators. Regarding claim 31 , Yu et al. disclose a second gate insulator disposed on the floating gate; and a control gate disposed on the second gate insulator and overlapping the floating gate. Regarding claim 33 , Yu et al. disclose a second gate insulator disposed on the floating gate; and a control gate disposed on the second gate insulator and overlapping the floating gate. Regarding claim 34 , Yu et al. disclose a substrate; a first isolation region disposed in the substrate and defining a recess that is bounded by the first isolation region on at least two sides, the first isolation region having a first depth beneath the recess and a second depth outward from the recess along at least one of the at least two sides, the first depth being greater

than or equal to the second depth; and a first conductor disposed in, and extending no higher than, the recess (see figure 7c). Regarding claim 35 , Yu et al. disclose the first and second insulators (316-318) respectively comprise first and second projections that define the recess (see figure 7c). Regarding claim 36 , Yu et al. disclose first and second trenches disposed in the substrate; and wherein the insulator is respectively disposed in the trench (see figure 7c). Regarding claim 36, the first conductor will inherently have some resistance therefore it inherently is a resistor. Regarding claim 37, the first conductor is separated from another conductive material (312) by an insulator therefore it inherently is a plate of a capacitor. Regarding claim 39 , Yu et al. disclose a first isolation region disposed in the substrate and defining a recess that is bounded by the first isolation region on at least two sides, the first isolation region having a first depth beneath the recess and a second depth outward from the recess along at least one of the at least two sides, the first depth being .greater than or equal to the second depth; a first conductor disposed in the recess; a second insulator disposed on the first conductor; and a second conductor (312) disposed on the second insulator (310) and overlapping the first conductor (see figure 7a and 7b). Regarding claim 49 , Yu et al. disclose a substrate having an active region; first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region and over a portion of at least one of the first and second insulators; a body region of a memory cell disposed in the portion of the active region; a first gate insulator disposed over the body region; and a floating gate of the memory cell disposed in the recess over the gate insulator and over the portion of one of the insulators (see figures 7a -7c).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sugihara (US 2002/0009815) disclose a planar control gate with a planar floating gate [0002].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bradley K Smith/
Primary Examiner, Art Unit 2891